What is claimed is:

1. A diode comprising:

a second conductive type impurity region formed by diffusing a second conductive type impurity of high concentration on a front surface of a silicon substrate having a first conductive type impurity of low concentration;

a first conductive type impurity region formed by diffusing a first conductive type impurity of high concentration on the front surface of the silicon substrate so as to surround the second conductive type impurity region with a predetermined width of a separation area apart from the second conductive type impurity region;

an interlayer dielectric formed so as to cover the front surface of the silicon substrate on which the first and second conductive type impurity regions are formed;

a first metal interconnect layer formed on the second conductive type impurity region and the separation area through the interlayer dielectric and electrically connected to the second conductive type impurity region through a connecting hole disposed the interlayer dielectric; and

a second metal interconnect layer formed so as to almost fully cover the first conductive type impurity region through the interlayer dielectric and electrically connected to the first conductive type impurity region through a connecting hole disposed in the interlayer dielectric.

2. The diode according to claim 1, wherein the first metal interconnect layer is formed so as to fully cover a border area between the first conductive type impurity region and the separation area through the interlayer dielectric.

3. A diode comprising:

a second conductive type impurity region formed by diffusing a second conductive type impurity of high concentration on a front surface of a silicon substrate having a first conductive type impurity of low concentration;

a first conductive type impurity region formed by diffusing a first conductive type impurity of high concentration on the front surface of the silicon substrate so as to surround the second conductive type impurity region with a predetermined width of a separation area apart from the second conductive type impurity region;

an electrode formed in the front surface of the separation area of the silicon substrate through an insulating film;

an interlayer dielectric formed so as to cover the front surface of the silicon substrate on which the first and second conductive type impurity regions and the electrode are formed;

a first metal interconnect layer formed on the second conductive type impurity region through the interlayer dielectric and electrically connected to the second conductive type impurity region and the electrode through a connecting hole disposed in the interlayer dielectric; and

a second metal interconnect layer formed so as to almost fully cover the first conductive type impurity region through the interlayer dielectric and electrically connected to the first conductive type impurity region through a connecting hole disposed in the interlayer dielectric.

4. The diode according to claim 3, wherein the electrode is formed as a predetermined distance apart from the first conductive type impurity region.